

FIG. 1(PRIOR ART)

FIG. 1(PRIOR ART)

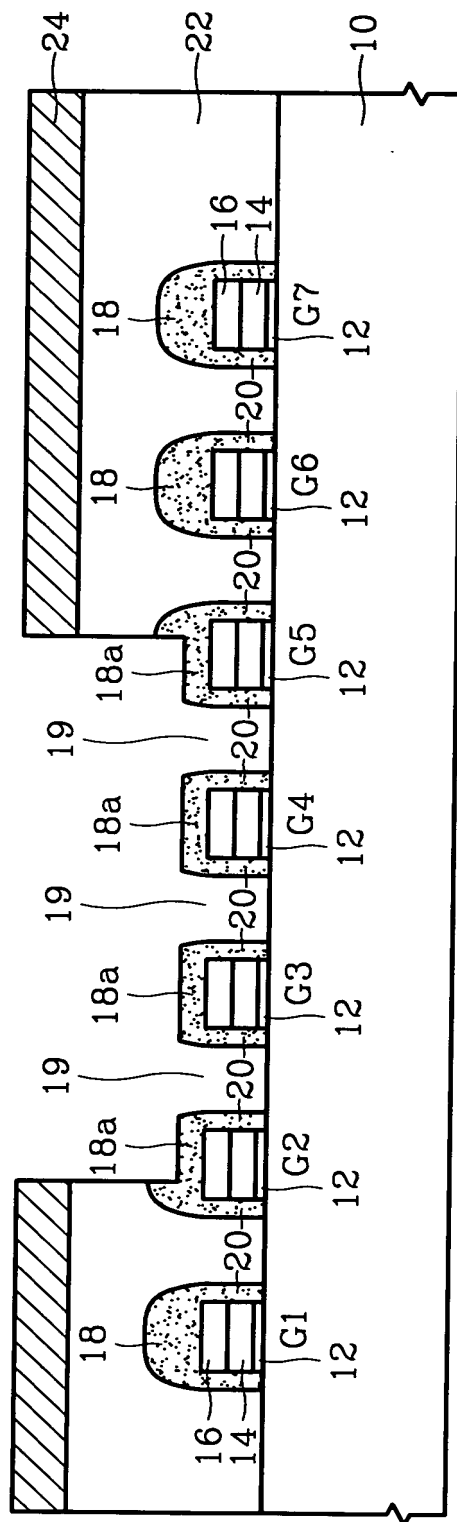


FIG. 2 is a cross-sectional view of a prior art device, showing a substrate 10 with a series of gates G1 through G7. Each gate is formed by a gate dielectric 12 and a gate electrode 14. A channel layer 16 is formed on top of the gate electrodes. A source/drain layer 18 is formed on top of the channel layer. A passivation layer 20 is formed on top of the source/drain layer. A top layer 22 is formed on top of the passivation layer. A bottom layer 26 is formed on top of the top layer.

FIG. 2(PRIOR ART)

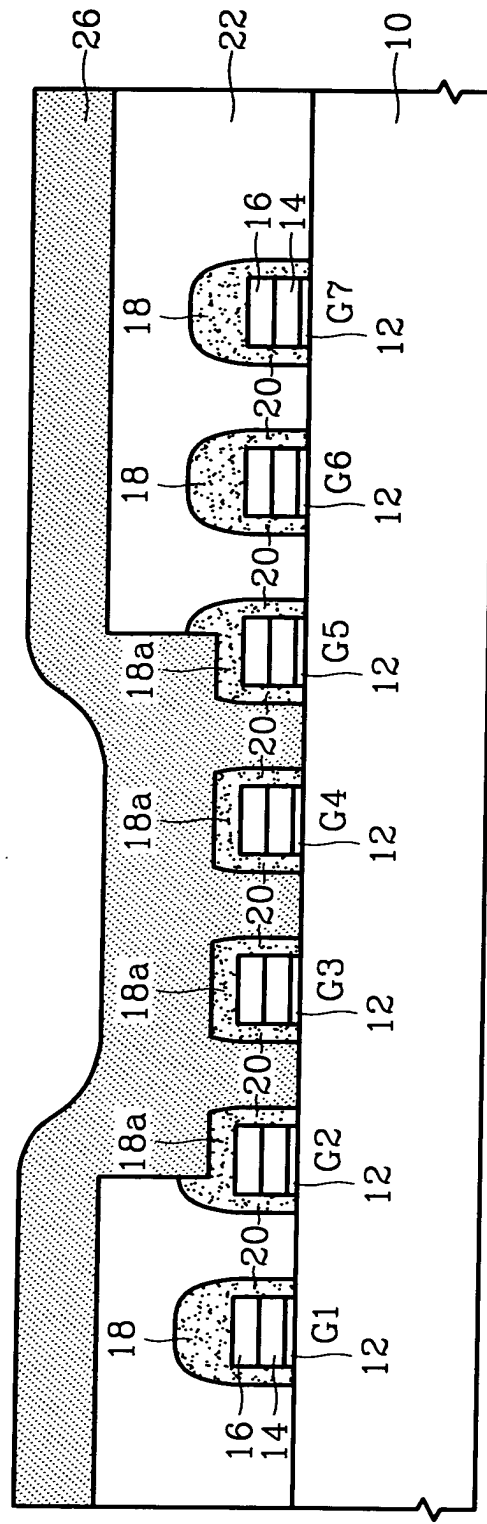


FIG. 3(PRIOR ART)

